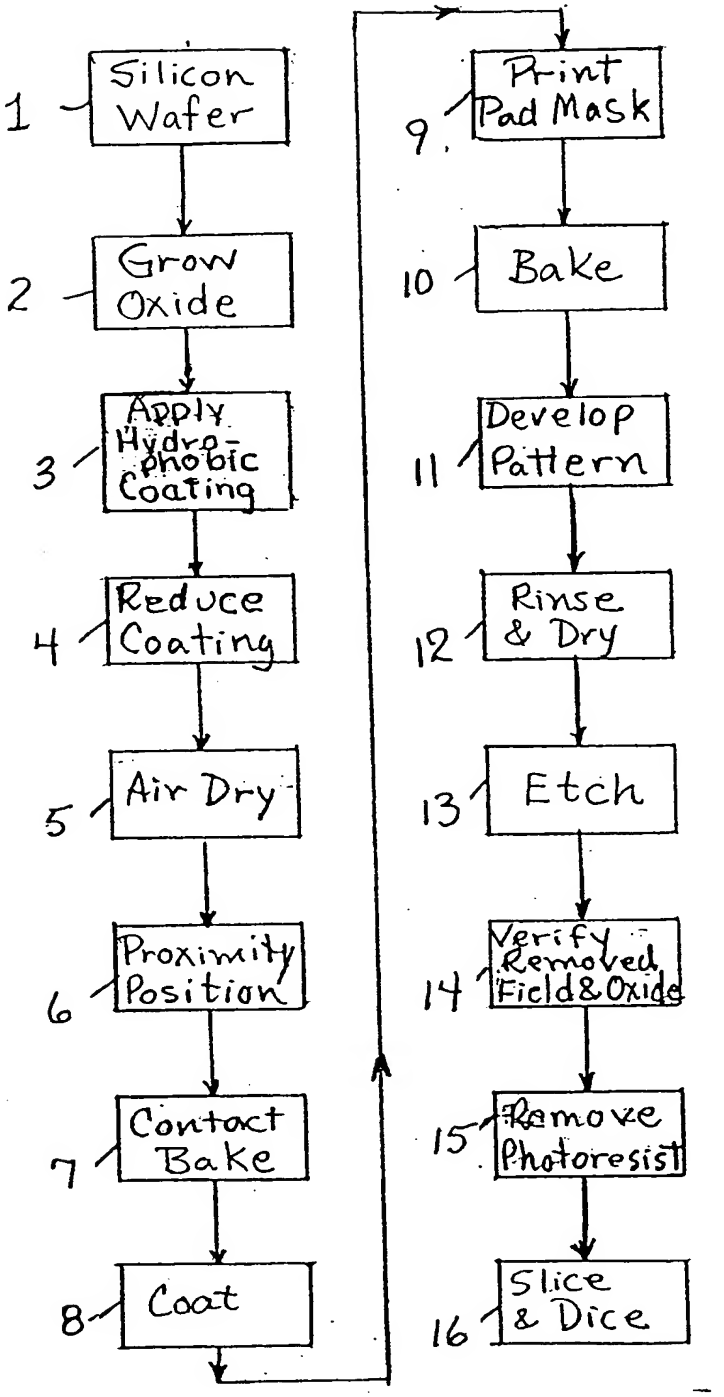
1
Silicon Wafer
2
Grow Oxide
3
Apply Hydro-phobic Coating
4
Reduce Coating
5
Air Dry
6
Proximity Position
7
Contact Bake
8
Coat
9
Print Pad Mask
10
Bake
11
Develop Pattern
12
Rinse & Dry
13
Etch
14
Verify Removed Field&Oxide
15
Remove Photoresist
16
Slice & Dice

FIG. 1

Cytonix Coat Process

Equipment - SVG 90 Series Track

3

Cytonix FLW. (Coat and Bake)					
Step	**Operation**	**Time (sec)**	**Speed (rpm)**	**Accel. (rpm/s)**	**Exhaust**
1	SPIN	3.0	2400	5000	20
2	DISP - 2	2.0	2400	5000	20
3	SPIN	30.0	2400	5000	20
4	SPIN	1.0	600	5000	50
5	BEBR1	8.0	600	5000	50
6	TEBR	6.0	1600	5000	50
7	SPIN	10.0	2000	5000	50
8	END				

7

High Temperature Bake - 180C		
Step	Time (sec)	X Pos (mm)
1	100.0	10.0
2	200	6
3	300	4
4	300	0

FIG. 2

MASK 2 - 96/384 Pad Mask

Critical Operating Parameters

Equipment - MTI FlexiFab (serial # 62-E1-2453)

Coat recipe

STEP	TIME	SPEED	ACCEL
1	002.0	00000	05
2	002.0	01200	05
3	000.3	01200	05
4	20.0	2000*	05
5	005.0	01000	05
6	010.0	02000	05
7	010.0	01300	05

**(Target RPM for desired thickness)*

Positive Resist Process

Photoresist: Shipley 1811 or 1822
Target thickness - 2.0um +/- .2um
Soft-Bake: 60" @ 105°C
Expose 96/384 Pad @ 350mj/cm²
Post Exposure Bake: 60" @ 115°C

Soft-bake - Hotplate Recipe

STEP	TIME	TEMP	HEIGHT
1	001.0	105°	0.026
2	060.0	105°	0.000

PEB - Hotplate Recipe

STEP	TIME	TEMP	HEIGHT
1	001.0	115°	0.026
2	060.0	115°	0.000

Positive Develop Process

Developer: Shipley MIF 701
Develop Time: 60"
Rinse/Dry

FIG. 3

Cross Section of Cytonix Chip: Pad Area Etched to Oxide

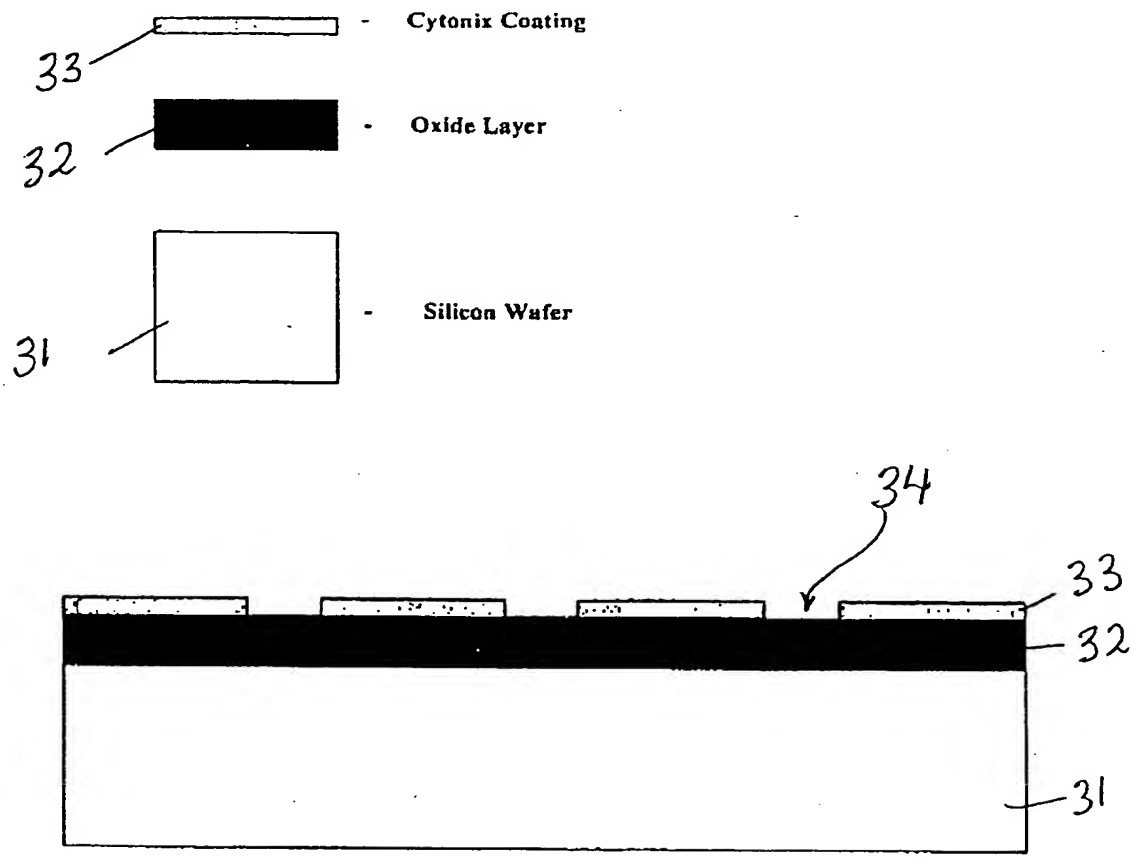

FIG.4